AMENDMENTS TO THE CLAIMS

Please cancel claims 1-6 and 13-14 and amend claims 7 to 12 and 15 to 17 as shown below. A complete listing of all pending claims is shown below.

1-6. (Cancelled)

7. (Currently amended) A clock supply circuit supplying a processing clock signal for processing an input signal having a predetermined frequency, said clock supply circuit comprising:

a clock generating means generating a intermediate clock signal for processing said input signal, a first clock signal higher in frequency than the intermediate clock signal, and a second clock signal lower in frequency than the intermediate clock signal,

a clock switching means selecting any of the intermediate clock signal, the first clock signal or the second clock signal, supplying the selected one as said processing clock signal to the signal processing, and

a clock switching control means for processing said input signal with use of the selected processing clock signal, detecting an amount out-of-sync of the processing clock signal with respect to the input signal in accordance with the processing result, and controlling the clock switching in accordance with said detected amount out-of-sync,

wherein said clock generating means further comprises:

an oscillation means generating a reference clock signal having a predetermined reference frequency,

a multiplying means generating a multiplied clock signal obtained by multiplying said reference clock signal, and

a frequency division means for dividing said multiplied clock signal by different frequency division ratios to generate said intermediate clock signal, said first clock signal and said second clock signal, respectively [A clock supply circuit as set forth in claim 6], and

wherein the clock switching means switches said clock signals using a predetermined time span as a switching time unit wherein at the start and ending time phases of said intermediate clock signal, said first and second clock signals match.

8. (Original) A clock supply circuit as set forth in claim 7, further comprises a counter for counting said multiplied clock signal, having a maximum count value set in accordance with a least common multiple of an intermediate division ration for generating said intermediate clock signal, a first division ratio for generating said first clock signal and a second division ratio for generating said second clock signal, wherein

said clock switching means performs clock switching when the count value of said counter reaches a predetermined value.

9. (Original) A clock supply circuit as set forth in claim 8, wherein said predetermined value is zero or said maximum count value.

10. (Currently Amended) A clock supply circuit as set forth in claim 5, wherein

said clock switching means switches said intermediate clock signal and said first clock signal using a predetermined time span as a first time switching unit wherein [at] the start and ending time phases of said intermediate clock signal and said first clock signal match, and

switches intermediate clock signal and said second clock signal using a predetermined time span as a second time switching unit wherein [at] the start and ending time phases of said intermediate clock signal and said second clock signal match.

11. (Original) A clock supply circuit as set forth in claim 10, further comprises

a first counter counting said multiplied clock signal, having a first maximum count value set in accordance with a least common multiple of an intermediate division ratio for generating said intermediate clock signal and a first division ratio for generating said first clock signal, and

a second counter counting said multiplied clock signal, having a second maximum count value set in accordance with a least common multiple of a intermediate division ration for generating said intermediate clock signal and a second division ratio for generating said second clock signal., wherein

said clock switching means further comprises

a first switching circuit performing clock switching of the intermediate clock signal and the first clock signal when the count value of said first counter reaches a first value, and

a second switching circuit performing clock switching of the intermediate clock signal and the second clock signal when the count value of said second counter reaches a second value.

12. (Currently Amended) A clock supply circuit as set forth in claim 11 wherein said first value is zero or said first maximum value, and said second value is zero or said second maximum value.

13-14. (Cancelled)

15. (Currently Amended) A clock supply circuit supplying a processing clock signal for processing an input signal having a predetermined frequency, said clock supply circuit comprising:

a clock generating means generating a first clock signal and a second clock signal having a lower frequency than that of said first clock signal,

a clock switching means selecting any of the first clock signal or the second clock signal, supplying the selected one as said processing clock signal to the signal processing, and

a clock switching control means for processing said input signal with use of the selected processing clock signal, detecting an amount out-of-sync of the processing clock signal with respect to the input signal in accordance with the processing result, and controlling the clock switching in accordance with said detected amount out-of-sync,

wherein said clock generating means further comprises:

an oscillation means generating a reference clock signal having a predetermined reference frequency,

a multiplying means generating a multiplied clock signal obtained by multiplying said reference clock signal, and

a frequency division means for dividing said multiplied clock signal by different frequency division ratios to generate said first clock signal and said second clock signal, respectively [A clock supply circuit as set forth in claim 14], and wherein

the clock switching means switches said clock signals using a predetermined time span as a switching time unit wherein [at] the start and ending time phases of said first and second clock signals match.

16. (Original) A clock supply circuit as set forth in claims 15, further comprises a counter for counting said multiplied clock signal, having a maximum count value set in accordance with a least common multiple of a first division ratio for generating said first clock signal and a second division ratio for generating said second clock signal, wherein

said clock switching means performs clock switching when the count value of said counter reaches a predetermined value.

17. (Original) A clock supply circuit as set forth in claim 16, wherein said predetermined value is zero or said maximum count value.